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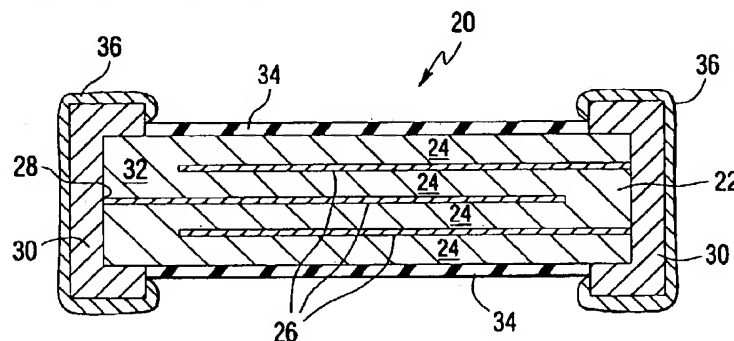
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(54) **Zinc phosphate coating for varistor and method**

(57) A method of providing a semiconductor device (20) with an inorganic electrically insulative layer (34) the device having exposed semiconductor surfaces (34) and electrically conductive metal end terminations (30) in which the device is reacted with phosphoric acid to form a phosphate on the exposed surfaces (34) of the

semiconductor but not on the metal end terminations (30), and in which the device is thereafter barrel plated in a conventional electrical barrel plating process and the plating is provided only on the end terminations (30) because the phosphate is not electrically conductive.



**FIG. 2**

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## Description

The present invention relates to nonlinear resistive devices, such as varistors, and more particularly to methods of making such devices using barrel plating techniques in which only the electrically contactable end terminals of the device are plated.

Nonlinear resistive devices are disclosed in the specifications of U.S. Patent No. 5,115,221.

Figure 1 is a typical device 10 that includes plural layers 12 of semiconductor material with electrically conductive electrodes 14 between adjacent layers. A portion of each electrode 14 is exposed in a terminal region 16 so that electrical contact may be made therewith. The electrodes 14 may be exposed at one or both of opposing terminal regions, and typically the electrodes are exposed at alternating terminal regions 16 as illustrated. The exposed portions of the electrodes 14 are contacted by electrically conductive end terminals 18 that cover the terminal regions 16.

The apparently simple structure of such devices belies their manufacturing complexity. For example, the attachment of the end terminals 18 has proved to be a problem in search of a solution. The terminal regions may be plated with nickel and tin-lead metals to increase solderability and decrease solder leaching. One method of affixing the end terminals 18 is to use a conventional barrel plating method in which the entire device is immersed in a plating solution. However, the stacked layers are semiconductor material, such as zinc oxide, that may be conductive during the plating process so that the plating adheres to the entire surface of the device. Thus, in order to provide separate end terminals as shown in Figure 1, a portion of the plating must be removed after immersion, or covered before immersion with a temporary plating resist comprised of an organic substance insoluble to the plating solution. However, the removal of the plating or organic plating resist is an extra step in the manufacturing process, and may involve the use of toxic materials that further complicate the manufacturing process.

It has also been suggested that the metal forming the end terminals 18 be flame sprayed onto the device, with the other portions of the surface of the device being masked. Flame spraying is not suitable for many manufacturing processes because it is slow and includes the creation of a special mask, with the additional steps attendant therewith, as disclosed in the specification of U.S. Patent No. 4,316,171.

An object of the present invention is to provide a method and device that obviates the problems of the prior art, and in which an electrically insulating, inorganic layer is formed on portions of the device before the device is barrel plated.

Another object is to provide a method and device in which a phosphoric acid is reacted with the exposed surface of stacked zinc oxide semiconductor layers to form a zinc phosphate coating, and in which a zinc phosphate coating protects portions of the device that

are not to be plated when the end terminals are formed.

A further object is to provide a method and nonlinear resistive device having a body of layers of semiconductor material with an electrode between adjacent layers, in which the body of the nonlinear resistive device is coated with an inorganic layer that is electrically insulating, except at a terminal region of the body where an electrode is exposed for connection to an end terminal, and in which the coated body is plated with an electrically conductive metal to form the end terminal in a process in which the body becomes electrically conductive and in which the electrically conductive metal does not plate the coated portions of the body because the inorganic layer is not electrically conductive.

The present invention includes a method of making a nonlinear resistive device comprising the steps of:

- (a) providing a body for the nonlinear resistive device, the exterior of the body being a zinc oxide semiconductor except at a terminal region where an end termination is provided;
- (b) reacting a phosphoric acid with the body to form an electrically insulative zinc phosphate coating on the exposed zinc oxide semiconductor, the end termination not being coated with the zinc phosphate; and
- (c) barrel plating the body to plate the end termination with an electrically conductive metal, wherein the electrically conductive metal does not form on the zinc phosphate coated portions of the body during the barrel plating because the zinc phosphate is not electrically conductive.

The invention also includes a method of providing an electrically insulative coating for a varistor, the method comprising the steps of:

- (a) providing an uncoated varistor having plural zinc oxide layers with electrodes therebetween, the electrodes contacting at least one of two exterior electrically conductive metal end terminations that are separated by an exposed surface of the zinc oxide layers;
- (b) submerging the uncoated varistor in a phosphoric acid solution for 25 to 35 minutes at 70°C to 80°C to form an electrically insulative zinc phosphate coating on the exposed surface of the zinc oxide layers, the end terminations not being coated with the zinc phosphate coating; and
- (c) subjecting the coated varistor to a barrel plating process in which the varistor is electrically charged and an electrically conductive plating material adheres to the charged portions of the varistor, the end terminations being plated and the zinc phosphate coating not being plated.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a pictorial depiction of a varistor typical of the prior art.

Figure 2 is vertical cross section of an embodiment of the device of the present invention.

Figure 3 is a pictorial depiction of a high energy disc varistor with an insulating layer of the present invention thereon.

Figure 4 is a pictorial depiction of a surface mount device with an insulating layer of the present invention.

Figure 2 illustrates an embodiment of a nonlinear resistive element 20 that includes a body 22 having stacked zinc oxide semiconductor layers 24 with planar electrodes 26 between adjacent pairs of layers 24. Each electrode 26 has a contactable portion 28 that is exposed for electrical connection to electrically conductive metal (preferably silver, silver-platinum, or silver-palladium) end terminations 30 that cover terminal regions 32 of the body 22 and contact the electrodes 26. The portions of body 22 not covered with the end terminations 30 are coated with an electrically insulative zinc phosphate layer 34. The end terminations 30 may be plated with layers 36 of electrically conductive metal that form electrically contactable end portions for the resistive element 20. By way of example, in one embodiment the zinc oxide layers 24 may have the following composition in mole percent: 94-98% zinc oxide and 2-6% of one or more of the following additives; bismuth oxide, cobalt oxide, manganese oxide, nickel oxide, antimony oxide, boric oxide, chromium oxide, silicon oxide, aluminum nitrate, and other equivalents.

The body 22 and end terminations 30 are provided conventionally. The zinc phosphate layer 34 may be formed by reacting phosphoric acid with the zinc oxide semiconductor layers exposed at the exterior of the body 22. The reaction may take place for 25-35 minutes at 70° to 80°C. By way of example, one part orthophosphoric acid (85 wt%) may be added to fifty parts deionized water. The solution may be heated to 75°C and stirred. The body 22 with end terminations 30 affixed may be washed with acetone and dried at 100°C for ten minutes. The washed device may be submerged in the phosphoric acid solution at 75°C for thirty minutes to provide the layer 34. After the layer 34 is applied, the body may be cleaned with hot, deionized water and dried at about 100°C for about fifteen minutes. The layer 34 does not adhere to the end terminations 30 because the silver or silver-platinum in the end terminations 30 is not affected by the phosphoric acid. The phosphoric acid solution may also be applied by spraying, instead of submerging, the washed device.

After the zinc phosphate layer 34 has been applied, the device may be barrel plated with an electrically conductive metal, such as nickel and tin-lead, to provide the layers 36. A conventional barrel plating process may be used, although the pH of the plating solution is desirably kept between about 4.0 and 6.0. In the barrel plating process the device is made electrically conductive and

the plating material adheres to the electrically charged portions of the device. The metal plating of layers 36 does not plate the zinc phosphate layer 34 during the barrel plating because the zinc phosphate is not electrically conductive.

The zinc phosphate layer 34 is electrically insulating and may be retained in the final product to provide additional protection. The layer 34 does not effect the I-V characteristics of the device.

In an alternative embodiment, the phosphate layer may be an inorganic oxide layer formed by the reaction of phosphoric acid with the metal oxide semiconductor in the device. For example, instead of zinc oxide, the semiconductor may be iron oxide, a ferrite, etc.

In another alternative embodiment, the method described above may be used in the manufacture of other types of electronic devices. For example, a high energy disc varistor has a glass or polymer insulating layer on its sides. With reference to Figure 3, instead of glass or polymer, the disc varistor 40 may have an insulating layer 42 of phosphate formed in the manner discussed above. The present invention is applicable to other varistor products such as a surface mount device depicted in Figure 4, radial parts, arrays, connector pins, discoidal construction, etc.

A method of providing a semiconductor device with an inorganic electrically insulative layer, the device having exposed semiconductor surfaces and electrically conductive metal end terminations. The device is reacted with phosphoric acid to form a phosphate on the exposed surfaces of the semiconductor but not on the metal end terminations. Thereafter barrel plated in a conventional electrical barrel plating process and the plating is provided only on the end terminations.

## Claims

1. A method of making a nonlinear resistive device comprising the steps of:

- (a) providing a body for the nonlinear resistive device, the exterior of the body being a zinc oxide semiconductor except at a terminal region where an end termination is provided;
- (b) reacting a phosphoric acid with the body to form an electrically insulative zinc phosphate coating on the exposed zinc oxide semiconductor, the end termination not being coated with the zinc phosphate; and
- (c) barrel plating the body to plate the end termination with an electrically conductive metal, wherein the electrically conductive metal does not form on the zinc phosphate coated portions of the body during the barrel plating because the zinc phosphate is not electrically conductive.

2. A method as claimed in claim 1 wherein the end termination comprises a layer of a metal selected from

the group consisting of silver, silver-platinum, and silver-palladium.

3. A method as claimed in claim 1 or 2 wherein the body comprises in mole percent, 94-98% zinc oxide and 2-6% of one or more of the additives selected from the group of additives consisting of bismuth oxide, cobalt oxide, manganese oxide, nickel oxide, antimony oxide, boric oxide, chromium oxide, silicon oxide, and aluminum nitrate. 5
4. A method as claimed in any one of claims 1 to 3 wherein the step of reacting phosphoric acid comprises the step of submerging the body in the phosphoric acid, with the step of submerging the body comprising the step of submerging the body in a orthophosphoric acid solution for 25 to 35 minutes at 70° to 80°C. 10
5. A method as claimed in any one of claims 1 to 4 wherein the electrically conductive metal comprises at least one of nickel and tin-lead, and the body is a varistor. 15
6. A method of providing a semiconductor device as claimed in any claims 1 to 5 including an inorganic electrically insulative layer, the semiconductor device having an exposed semiconductor surface and electrically conductive metal end terminations, the method comprising the steps of: 20
  - (a) exposing the semiconductor device to a phosphoric acid solution to form a phosphate coating on the exposed semiconductor surfaces, and not on the end terminations; and 25
  - (b) barrel plating the semiconductor device with an electrically conductive metal plating in a process in which the device is electrically charged and submerged in a plating solution, the plating being formed on the end terminations and not on the phosphate coating because the phosphate coating is not electrically conductive. 30
7. A method as claimed in claim 6 wherein the exposed semiconductor surfaces comprise one of zinc oxide and iron oxide. 35
8. A method as claimed in claims 6 or 7 wherein the phosphoric acid solution comprises orthophosphoric acid and deionized water. 40
9. A nonlinear resistive element made by the process of any one of claims 6 to 8. 45
10. A method of providing an electrically insulative coating for a varistor, the method comprising the steps of: 50

(a) providing an uncoated varistor having plural zinc oxide layers with electrodes therebetween, the electrodes contacting at least one of two exterior electrically conductive metal end terminations that are separated by an exposed surface of the zinc oxide layers;

(b) submerging the uncoated varistor in a phosphoric acid solution for 25 to 35 minutes at 70°C to 80°C to form an electrically insulative zinc phosphate coating on the exposed surface of the zinc oxide layers, the end terminations not being coated with the zinc phosphate coating; and

(c) subjecting the coated varistor to a barrel plating process in which the varistor is electrically charged and an electrically conductive plating material adheres to the charged portions of the varistor, the end terminations being plated and the zinc phosphate coating not being plated.

#### 11. A nonlinear resistive element comprising:

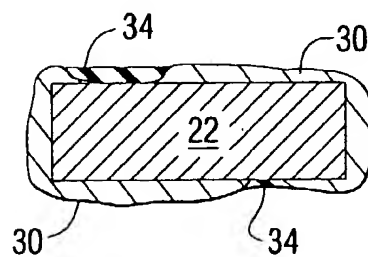
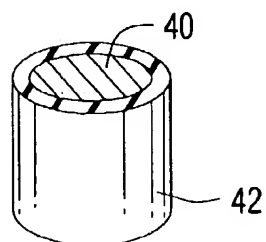
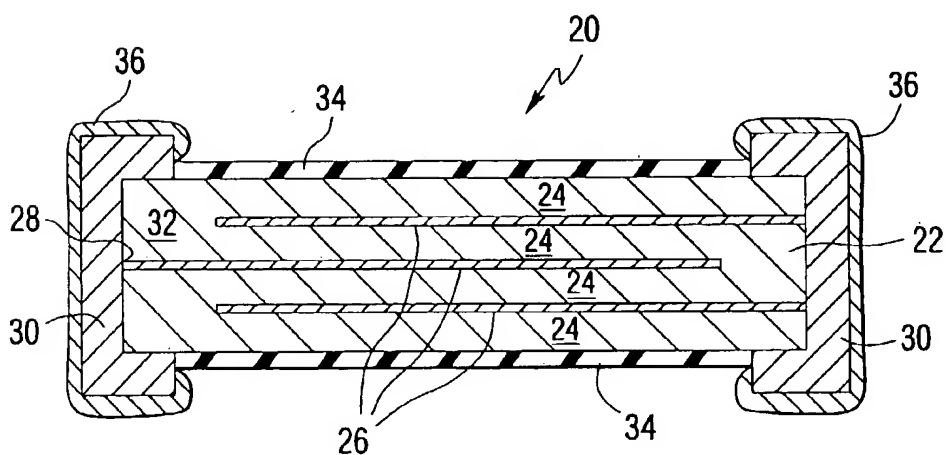
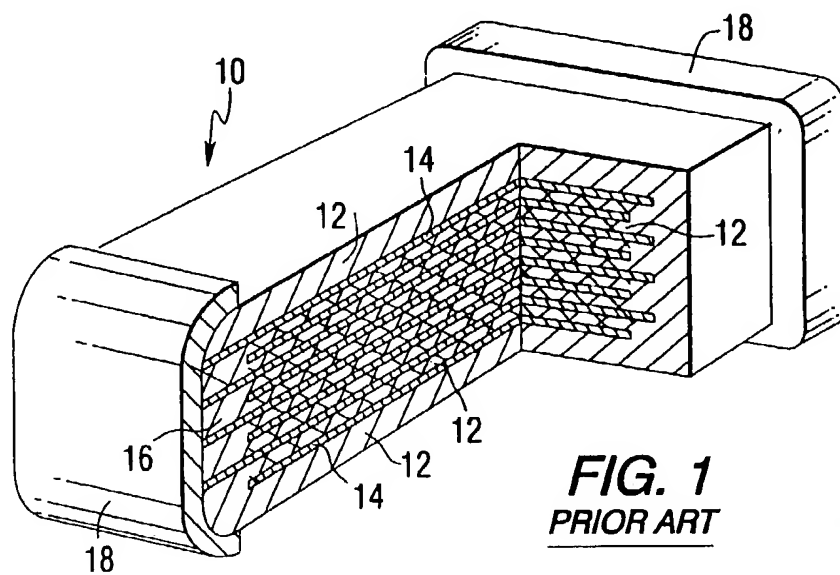
a body constituted by a varistor having stacked zinc oxide semiconductor layers;

a planar electrode between each pair of said layers, each said electrode having a contactable portion that is exposed for electrical connection;

plural spaced electrically conductive metal end terminations, each of said end terminations being on an end portion of said body for contacting at least one said contactable portion;

an electrically insulative zinc phosphate coating covering said body between said end terminations;

a metal plating covering said end terminations, and in which the body comprises in mole percent, 94-98% zinc oxide and 2-6% of one or more of the additives selected from the group of additives consisting of bismuth oxide, cobalt oxide, manganese oxide, nickel oxide, antimony oxide, boric oxide, chromium oxide, silicon oxide, and aluminum nitrate.





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# EUROPEAN SEARCH REPORT

Application Number  
EP 96 40 0993

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 303 (E-1228), 3 July 1992 & JP 04 083302 A (TOSHIBA CORP), 17 March 1992, * abstract *	1,10,11	H01C1/034 H01C7/10
A	--- PATENT ABSTRACTS OF JAPAN vol. 015, no. 343 (E-1106), 30 August 1991 & JP 03 131004 A (TOSHIBA CORP), 4 June 1991, * abstract *	1,10,11	
A	--- GB 2 100 246 A (ARMSTRONG WORLD IND INC) 22 December 1982 * the whole document *	1,10,11	
A	--- PATENT ABSTRACTS OF JAPAN vol. 014, no. 016 (E-872), 12 January 1989 & JP 01 259506 A (ROHM CO LTD), 17 October 1989, * abstract *	1,5,10	
A	--- PATENT ABSTRACTS OF JAPAN vol. 017, no. 514 (E-1433), 16 September 1993 & JP 05 136012 A (ROHM CO LTD), 1 June 1993, * abstract *	1,10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01C
A,D	--- US 5 115 221 A (COWMAN STEPHEN P) 19 May 1992 * the whole document *	1-3	
A	--- GB 2 044 531 A (TDK ELECTRONICS CO LTD) 15 October 1980 * the whole document *	15 1	
D	& US 4 316 171 A (MIYABAYASHI ET AL.) * the whole document *		
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 4 November 1996	Examiner Lina, F
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons</p> <p>&amp; : member of the same patent family, corresponding document</p>			

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Application Number  
EP 96 40 0993

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
E	EP 0 716 429 A (HARRIS CORP) 12 June 1996 * the whole document * -----	1-11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 4 November 1996	Examiner Lina, F
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X : particularly relevant if taken alone  Y : particularly relevant if combined with another document of the same category  A : technological background  O : non-written disclosure  P : intermediate document</p> <p>T : theory or principle underlying the invention  E : earlier patent document, but published on, or after the filing date  D : document cited in the application  I : document cited for other reasons</p> <p>.....  &amp; : member of the same patent family, corresponding document</p>			

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